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10/092,166	03/04/2002	Afshin Momtaz	BU2138	9226

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EXAMINER	
WONG, LINDA	
ART UNIT	PAPER NUMBER
2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/092,166	MOMTAZ ET AL.	
	Examiner	Art Unit	
	Linda Wong	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10 and 14* is/are allowed.

6)☒ Claim(s) *1-9,11-13,15-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response to Arguments

1. Applicant's arguments filed have been fully considered but they are not persuasive.

2. The applicant contends

" Claim 1 requires a "delay circuit [that] is configured to shift the phase of the incoming data signal in a manner that is symmetrical with respect to a sampling edge of the clock signal." Claims 2, 4, and 20 also require a symmetrical delay between the clock and data signals. As explained in the specification, the delay circuit is configured to delay the incoming data signal in this manner so that a single flip-flop can be used in the circuit to detect bit errors. When the extracted CLK signal is loaded down by only a single flip-flop like this, the capacitive load on the high-speed signal path is minimized, such that the claimed loss-of-signal detector can be used with high speed communications standards (e.g., SONET, ATM), e.g., at speeds greater than 10 Gb/s, even when CMOS devices are used. See Application at paragraphs 21, 18, and 17. The Office action does not cite any reference as disclosing the claimed "delay circuit [that] is configured to shift the phase of the incoming data signal in a manner that is symmetrical with respect to a sampling edge of the clock signal," but asserts "it is well known in the art to symmetrically delay the incoming data and it would be obvious to one skilled in the art to perform such a task to avoid error before and after the sampled edge." Office action at page 3. Respectfully, the Office fails to establish a prima facie case of obviousness because the Office fails to provide a motivation to include a symmetric delay with the other elements of the claim. Without agreeing with the statements in the Office action, even if a symmetric delay would "avoid error before and after the sampled edge," this still provides no motivation to combine this feature with other elements of the claim, since there are plenty of other ways of avoiding error before and after a sampled edge: Just because it is possible to combine features from different references does not mean that a motivation to do so exists. As explained above, the symmetric delay is used so that only a single flip-flop is needed in the claimed loss-of-signal circuit, and by using only a single flip-flop capacitive loading on the signal line is reduced, which allows the circuit to be implemented in CMOS devices and used in high-speed applications. Moreover, the object of the claimed circuit is to detect errors in the timing between the extracted clock signal and the data signal, rather than to "avoid errors" as cited in the Office action.

Therefore, because claims 1, 2, 4, and 20 would not have been obvious, applicant respectfully requests allowance of these claims and their base claims."

3. The examiner respectfully disagrees. Regarding the limitation "the delay circuit configured to shift the phase of the incoming data in a manner that is symmetrical

with respect to a sampling edge of the clock signal", as stated in the office action "Pasqualini discloses a delayed data input, a received clock and a flip-flop for comparing the delayed data with the clock." The examiner has shown that the reference contains the recited limitation of a "delay circuit" which provides a delayed data signal. Furthermore, Whitt discloses a delay line for delaying the input signal and providing a delayed input signal into the phase detector. (Fig. 2, labels 10 and 84) It is well known in the art the amount of delay performed by the delay circuit depends on a predetermined delay period. Since the delay circuit can be adjusted or set to any predetermined delay period, the delay circuit inherently shifts the phase of the incoming signal depending on the set predetermined delay period. Both Pasqualini and Whitt show two types of delay circuits, wherein the amount of shift is dependent on the predetermined delay period. Pasqualini discloses a fixed predetermined delay, wherein the incoming signal is delayed by a period of time. (Col. 3, lines 1-25) Pasqualini further discloses in Fig. 9 a programmable delay circuit (Col. 8, lines 18-20) comprising a set of delays (Fig. 9, label 1116) and a flip-flop (Fig. 9, label 1118) for selecting or latching onto the delayed signal depending on the recovered clock signal (Fig. 9, labels 1124,1118,1116) Since the output of the delayed signal is dependent on the predetermined delay period or the delay circuit as shown in Fig. 9 and the recovered clock signal as shown in Fig. 9, the delayed output can be adjusted depending on the clocked signal and the predetermined delay. Furthermore, the output delay signal can be symmetrical to

the clocked signal depending on the recovered clocked signal and the predetermined delay as disclosed by Pasqualini.

4. Regarding the applicant's remarks on the motivation for combining the delay circuit as shown by Pasqualini into Whitt's invention, to show proper prima face plausibility and motivation for the combination must be shown. Whitt discloses a delay line for delaying the incoming signal. (Fig. 2, labels 10 and 84) Whitt further discloses "the delay line value of the delay line 84 of Fig. 2 can in principle be chosen arbitrarily..." (Col. 6, lines 49-51) This indicates the delay line as disclosed by Whitt can be set to delay the input signal by any predetermined delay period or amount. Thus, combining Whitt and Pasqualini is possible. The motivation to replace or incorporate the delay line as disclosed by Pasqualini into Whitt's invention depends on the designer's choice and the purpose for producing a delayed signal. The motivation as stated in the office action shows motivation for providing a delayed signal is to "avoid error before and after the sampled edge" and the designer's decision for setting the predetermined delay and recovering the clock signal. Furthermore, Pasqualini discloses "by choosing the appropriate number of delay stages to be employed, any amount of data delay can be obtained at any data rate". This indicates by delaying the input signal appropriately, the input signal can be received at any data rate. Thus, by combining Pasqualini's invention into Whitt's invention the delayed signal can increase robustness to Whitt's invention.

5. Regarding the applicant's remark: "As explained in the specification, the delay circuit is configured to delay the incoming data signal in this manner so that a single

flip-flop can be used in the circuit to detect bit errors. When the extracted CLK signal is loaded down by only a single flip-flop like this, the capacitive load on the high-speed signal path is minimized, such that the claimed loss-of-signal detector can be used with high speed communications standards (e.g., SONET, ATM), e.g., at speeds greater than 10 Gb/s, even when CMOS devices are used. See Application at paragraphs 21, 18, and 17.", such limitations are not recited in the claim.

6. Based on the above rebuttal, the rejections as stated in the previous office action stands. A copy of the rejection is included below.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. **Claims 1-6** are rejected under 35 U.S.C. 103(a) as being unpatentable over Whitt (US Patent No.: 4881243) in view of Schuur (US Patent No.: 5590157), further in view of Pasqualini (US Patent no.: 6397374) and further in view of Gailhard et al (US Patent No.: 6703880).

   a. **Claim 1**, Whitt a clock recovery circuit (Fig. 2, label 2) for extracting a recovered clock signal from an incoming data signal (Fig. 2, labels input, 10, ck, 70), a

phase detector (Fig.1, labels 30 and 20) or flip flop coupled to receive the recovered clock signal (Fig. 1, label 70 and clock signal) at one input and the data signal (Fig. 1, label 10) at a second input, an integrator coupled to an output of the flip-flop (Fig. 2, label 35), a comparator (Fig. 1, label 50) having a first input coupled to an output of the integrator (Fig. 1, label 35) and a second input coupled to a threshold voltage (Fig. 1, label 8). Although Whitt fails to show a switch for resetting the integrator, Schuur discloses an integrator comprising a switch for resetting. (Fig. 3A, label 8) It would be obvious to incorporate a switch to reset the integrator to discharge the integrator and allow for integration of different portion of the signal. Although Whitt fails to disclose receiving a delayed input data signal, Pasqualini discloses a delayed data input, a received clock and a flip-flop comparing the delayed data with the clock. It would be obvious to one skilled in the art to incorporate Pasqualini's invention to Whitt to allow delayed data waveform to make a complete voltage excursions from the ground voltage and the power supply so to prevent dependent hold violations from occurring. Although Pasqualini fails to disclose the delay circuit is configured to shift the phase of the incoming data signal in a manner that is symmetrical with respect to a sampling edge of the clock signal, it is well known in the art to symmetrically delay the incoming data and it would be obvious to one skilled in the art to perform such a task to avoid error before and after the sampled edge. Although Whitt fails to disclose the full details of the phase detector or flip-flop, wherein the flip-flop is configured to generate an error

signal when a transition of the delayed data signal falls outside of AT on either side of a falling edge of the recovered clock signal, Gailhard et al discloses a phase comparator for outputting error signals when the data signal is delayed before or after the clock signal for a change in period. (Fig. 1 and Fig. 2a-2d) It would be obvious to one skilled in the art to incorporate the phase comparator into the phase detector as disclosed by Whitt to provide a high frequency clock signal from a low frequency clock signal. (Col. 1, lines 18-20) Although Gailhard et al fails to discloses a specific difference in phase between the clock signal and data signal, it would be obvious to one skilled in the art to have a specific phase difference based on designer's choice.

b. **Claim 2** inherits all the limitations of claim 1, but claim 1 recites the limitation of (T/2)+/-deltaT. Although Gailhard et al fails to disclose such a limitation, Gailhard et al discloses detecting a variable amount of delay between the input signal and clock. It would be obvious to one skilled in the art to detect the delayed data falling outside such a range depending on designer's choice.

c. **Claim 3** inherits all the limitations of claim 1, but claim 1 does not recite the limitation of the delay period is substantially equal to about ¼. Although Gailhard et al fails to disclose such a limitation, Gailhard et al discloses detecting a variable amount of delay between the input signal and clock. It would be obvious to one skilled in the art to detect the delayed data falling outside such a range depending on designer's choice.

d. **Claim 4** inherits all the limitations of claim 1, but claim 1 does not recite the limitation of using C3MOS logic to build the delay circuit. C3MOS logic is a well known type of logic and it would be obvious to one skilled in the art to use such a type of logic based on designer's choice and to provide optimum balance between speed and power consumption.

e. **Claim 5** inherits all the limitations of claim 4.

f. **Claim 6,** Schuur discloses an integrator receiving the error signal from the phase detector (Fig. 2, labels 1 and 2) and the integrator outputs the frequency equal to the bit rate, wherein the frequency would also be related to the error rate depending on the output from the phase detector. (Col. 5, lines 35-36 and Fig. 2, labels 1 and 2)

8. **Claims 7-9,11-12** are rejected under 35 U.S.C. 103(a) as being unpatentable over Whitt (US Patent No.: 4881243) in view of Schuur (US Patent No.: 5590157), further in view of Pasqualini (US Patent no.: 6397374) and further in view of Gailhard et al (US Patent No.: 6703880) and further in view of Ten Pierick (US Patent No.: 6226344).

a. **Claim 7**, Although Schuur fails to disclose the elements in the integrator, Ten Pierick discloses an integrator comprising a current source configured to supply current Io (Fig. 3, label I), a capacitor (Fig. 3, label C) and a first switch (Fig. 3, label S1) coupled between the current source (Fig. 3, label I) and the capacitor (Fig. 3, label C), and configured to open or close in response to the error signal

(Fig. 3, label 2). Although Ten Pierick fails to disclose an error signal generated by the flip-flop, Schuur disclose such a limitation. (Fig. 2, labels 1 and 2) It would be obvious to one skilled in the art to incorporate the integrator as disclosed by Ten Pierick into Schuur's invention to generate a time period with very high accuracy using a simple method.

b. **Claim 8**,Ten Pierick discloses a second switch (Fig. 3, label S2) coupled in parallel to the capacitor (Fig. 3, label C) for discharging the capacitor in response to the timing generation circuit (Fig. 4, label 130 and Col. 6, lines 22-28). Although Ten Pierick fails to disclose a second switch controlled by the error outputted by the flip-flop, Schuur discloses a flip-flop (Fig. 2, label 1) outputting an error to the integrator (Fig. 2, label 2). It would be obvious to one skilled in the art to use the error signal to control the second switch based on designer's choice and to maximize use of dynamic range of the integration at different clock pulse frequencies. (Col. 6, lines 64-65)

c. **Claim 9**, Although Schuur fails to disclose the component in the integrator, Ten Pierick discloses an integrator outputting a voltage and a comparator (Fig. 3, label 4) compares the output from the integrator to a reference level. (Fig. 3, label 4 and Col. 6, lines 31-34) It would be obvious to one skilled in the art to incorporate the integrator as disclosed by Ten Pierick into Schuur's invention to generate a time period with very high accuracy using a simple method.

d. **Claim 11**, although Ten Pierick, Schuur fails to disclose using a pair of differentially coupled metal-oxide-semiconductor field effect transistors, it would

be obvious to one skilled in the art to build a switch using MOSFETs based on the designer's choice.

e. **Claim 12**, Although Ten Pierick, Schuur fails to disclose the pair of MOSFET are p-channel type, it would be obvious to one skilled in the art to use MOSFET p-channel type transistors based on the designer's choice.

9. **Claims 15,16** are rejected under 35 U.S.C. 103(a) as being unpatentable over Whitt (US Patent No.: 4881243) in view of Gailhard et al (US Patent No.: 6703880) and further in view of Peragine (US Patent No.: 6623185).

a. **Claim 15**, Whitt discloses a clock and data recovery block (Fig. 2, label 2) coupled to receiving an incoming data signal (Fig. 2, label 10) and configured to extract a recovered clock signal (Fig. 2, labels ck and 70) from the incoming data signal (Fig. 2, label 10), a static-loss-of-signal detector (Fig. 2, labels 84,80,85,56,60,20,30 and 35) to receive the incoming data signal (Fig. 2, label 10) and recovered clock signal (Fig. 2, labels 70 and ck) and configured to measure the bit error rate (Fig. 2, output from labels 35 and 85). Although Whitt fails to disclose the elements in the integrators, Ten Pierick discloses an integrator (Fig. 3, label 3) comprising a capacitor (Fig. 3, label C). It would be obvious to one skilled in the art to incorporate the integrator as disclosed by Ten Pierick into Whitt's invention to generate a time period with very high accuracy using a simple method. Although Whitt fails to disclose the full details of the phase detector or flip-flop, wherein the flip-flop is configured to generate

an error signal when a transition of the delayed data signal falls outside of AT on either side of a falling edge of the recovered clock signal, Gailhard et al discloses a phase comparator for outputting error signals when the data signal is delayed before or after the clock signal for a change in period. (Fig. 1 and Fig. 2a-2d) It would be obvious to one skilled in the art to incorporate the phase comparator into the phase detector as disclosed by Whitt to provide a high frequency clock signal from a low frequency clock signal. (Col. 1, lines 18-20) Although Gailhard et al fails to discloses a specific difference in phase between the clock signal and data signal, it would be obvious to one skilled in the art to have a specific phase difference based on designer's choice. Although Gailhard et al and Whitt fail to disclose a retiming circuit, Pergine discloses a clock data recovery (Fig. 2, labels 202,204,206,208) and a retiming circuit (Fig. 2, label 210) coupled to receiving the incoming data (Fig. 2, label data) and the recovered clock signal (Fig. 2, output from label 208) and configured to generate a retimed data signal (Fig. 2, label retimed data). It would be obvious to one skilled in the art to incorporate a retimed data signal component to detect lack of transitions to indicate LOS event, which provides better detect the performance of a receiver.

b. **Claim 16** inherits all the limitations of claim 15.

10. **Claims 17,21** are rejected under 35 U.S.C. 103(a) as being unpatentable over Whitt (US Patent No.: 4881243) in view of Schuur (US Patent No.: 5590157), further in

view of Pasqualini (US Patent no.: 6397374), further in view of Gailhard et al (US Patent No.: 6703880) and further in view of Peragine (US Patent No.: 6623185).

a. **Claim 17** inherits all the limitations of claim 3.

b. **Claim 21** inherits all the limitations of claim 3.

11. **Claims 18-19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Whitt (US Patent No.: 4881243) in view of Schuur (US Patent No.: 5590157), further in view of Pasqualini (US Patent no.: 6397374), further in view of Gailhard et al (US Patent No.: 6703880), further in view of Peragine (US Patent No.: 6623185) and further in view of Ten Pierick (US Patent No.: 6226344).

a. **Claim 18** inherits all the limitations of claims 7 and 8.

b. **Claim 19** inherits all the limitations of claims 7 and 8.

12. **Claims 20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Whitt (US Patent No.: 4881243) in view of Schuur (US Patent No.: 5590157), further in view of Pasqualini (US Patent no.: 6397374) and further in view of Gailhard et al (US Patent No.: 6703880).

a. **Claim 20** inherits all the limitations of claim 1, but claim 1 fails to recite the limitation integrating a plurality of error signals over a period of time. Whitt discloses a phase detector, which inherently, continuously outputs a plurality of error signals and integrating the outputs of the phase detector. (Fig. 2, labels 30 and 35)

Allowable Subject Matter

13. **Claims 10 and 14** are allowed over prior art.

Conclusion

14. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

15. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linda Wong whose telephone number is 571-272-6044. The examiner can normally be reached on 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Linda Wong

JAY K. PATEL
SUPERVISORY PATENT EXAMINER